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TDO 8/20/2007

Amendments to the Specification:

Please amend the Specification as follows.

Please insert the following at Page 3, line 1 of the original application, immediately preceding the paragraph beginning, "FIGURE 4 illustrates. . .":

"FIGURE 3A illustrates a timing diagram showing various signals of the preferred embodiment of FIGURE 3;"

Please insert the following at Page 9, line 29 of the original application, immediately preceding the paragraph beginning, "Now referring to FIGURE 4,. . .":

"Now referring to FIGURE 3A, the reference numeral 370 generally refers to a timing diagram showing various signals of the embodiment as illustrated in FIGURE 3. One skilled in the art will understand that the timing diagram describes the logic states of various signals over an operational time period. As such, one skilled in the art can derive a similar timing diagram based solely on FIGURE 3—depending on the skill of the artisan, a mental timing diagram can be derived that tracks the timing diagram offered in FIGURE 3A. Accordingly, the timing diagram illustrated in FIGURE 3A is offered as a visual aid to understanding, saving time for one skilled in the art seeking to understand the embodiment depicted in FIGURE 3.

Certain assumptions have been made in order to simplify description of the operation of the circuit in FIGURE 3. First, an arbitrary delay time has been selected that is approximately equal to one-half the pulse width of the input clock. Second, the "delay time" as depicted in FIGURE 3A refers to the time it takes for a high-to-low transition at node a0 to propagate through the delay blocks 320-326, through node a20 and inverter 328, to node na20. One skilled in the art will understand that other delay times can also be selected, as described in more detail below. Third, the particular signals shown have been somewhat simplified and depicted as perfectly formed square